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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/672,328	09/26/2003	Todd M. Witter	42P8015C	8420

7590 02/06/2006

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EXAMINER

TSAI, SHENG JEN

ART UNIT PAPER NUMBER

2186

DATE MAILED: 02/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.		Applicant(s)	
	10/672,328		WITTER ET AL.	
	Examiner		Art Unit	
	Sheng-Jen Tsai		2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 27 December 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-14 is/are pending in the application.
- 4a) Of the above claim(s) 2,3,10 and 11 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1,4-9 and 12-14 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____. |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date _____. | 6) <input type="checkbox"/> Other: _____. |

DETAILED ACTION

1. This Office Action is taken in response to Applicants' Amendment and Remarks filed on December 27, 2005 regarding application 10/672,328 filed on September 26, 2003.

2. Claims 1 and 9 have been amended.

Claims 2-3 and 10-11 have been cancelled.

Claims 1, 4-9 and 12-14 are pending in the application under consideration.

3. ***Response to Amendments and Remarks***

Independent claims 1 and 9 have been amended with new limitation of "a timer to insert a delay time between consecutive fragment requests for fragments from different planes."

Claims 1 and 9 become allowable with the amended limitation.

Double Patenting

4. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

5. Claims 1, 4-9 and 12-14 are rejected under the judicially created doctrine of anticipation-type double patenting as being anticipated by claims 1-6 of US patent **6,629,253** (Witter et al., "System for Efficient Management of memory Access Requirements from a Planar Video Overlay Data Stream Using a Time Delay"), as shown in the following table. Although not all of the conflicting claims are exactly identical, they are extremely similar and are not patentably distinct from each other as explained in the "explanation" column of the table below:

6,629,253	10/672,328
1. An apparatus comprising: a request unit to request more than one fragment of isochronous data from a memory device wherein the isochronous data is overlay data organized in the memory device into a first, a second, and a third plane of overlay data, the request unit to request fragments from the memory device in the sequence of from the first plane, then from the second plane, then from the third plane, the request unit to then repeat the sequence; a timer to insert a delay after requests for fragments from the first and second planes; and an additional timer to insert an additional delay after requests for fragments from the third plane.	1. (Currently amended) An apparatus, comprising: a request unit to request more than one fragment of isochronous data from a memory device, wherein the isochronous data is overlay data organized in the memory device as more than one plane of data; and a timer to insert a delay time between consecutive fragment requests for fragments from different planes.
2. The apparatus of claim 1, wherein the delay inserted by the timer is shorter than the delay	4. (Original) The apparatus of claim 1, wherein the isochronous data is overlay data organized in the memory

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inserted by the additional timer.	device into a first, a second, and a third plane of overlay data.
3. The apparatus of claim 2, wherein the timer and the additional timer are programmable.	5. (Original) The apparatus of claim 4, the request unit to request fragments from the memory device in the sequence of from the first plane, then from the second plane, then from the third plane, the request unit to then repeat the sequence.
4. A system comprising; a memory device; and a system logic device coupled to the memory device, the system logic device including an overlay data unit, the overlay data unit including a request unit to request more than one fragment of overlay data from the memory device wherein the overlay data is organized in the memory device into a first, a second, and a third plane of overlay data, the request unit to request fragments from the memory device in the sequence of from the first plane, then from the second plane, then from the third plane, the request unit to then repeat the sequence, a timer to insert a delay after requests for fragments from the first and second planes, and an additional timer to insert an additional delay after requests for fragments from the third plane.	6. (Original) The apparatus of claim 5, wherein the timer inserts a delay after requests for fragments from the first and second planes.
5. The system of claim 4, wherein the delay inserted by the timer is shorter than the delay inserted by the additional timer.	7. (Original) A method, comprising: organizing overlay data stored in a memory device into more than one plane; issuing multiple requests for overlay data fragments from the memory device where consecutive requests for overlay data fragments are requests for data from different planes; and inserting a delay between requests for overlay data fragments.
6. The system of claim 5, wherein the timer and the additional timer are programmable.	8. (Original) A method, comprising: organizing overlay data stored in a memory device into a first plane, a second plane, and a third plane; requesting an overlay data fragment from the first plane; inserting a delay after requesting the overlay data fragment from the first plane; requesting an overlay data fragment from the second plane; inserting a delay after requesting the overlay data fragment from the second plane; requesting an overlay data fragment from the third plane; and inserting a delay after requesting the overlay data fragment from the third plane.
	9. (Currently amended) A system, comprising: a memory device', and a system logic device coupled to the memory device, the system logic device including an overlay data unit, the overlay data unit including a request unit to request more than one fragment of overlay data from the memory device, wherein the overlay data is organized in the memory device as more than one plane of data; and a timer to insert a delay time between consecutive fragment requests for fragments from different planes.
	12. (Original) The system of claim 9, wherein the overlay data is organized in the memory device into a first, a second, and a third plane of overlay data.
	13. (Original) The system of claim 12, the request unit to request fragments from the memory device in the sequence of from the first plane, then from the second plane, then

	from the third plane, the request unit to then repeat the sequence.
	14. (Original) The system of claim 13, wherein the timer inserts a delay after requests for fragments from the first and second planes.

Allowable Subject Matter

6. Claims 1, 4-9 and 12-14 are rejected under the judicially created doctrine of anticipation-type double patenting as being anticipated by claims 1-6 of US patent 6,629,253, but would be allowable if able to overcome the double patenting rejections.

Conclusion

7. Claims 1, 4-9 and 12-14 are rejected as explained above.

Claims 1, 4-9 and 12-14 are rejected under the judicially created doctrine of anticipation-type double patenting as being anticipated by claims 1-6 of US patent 6,629,253, but would be allowable if able to overcome the double patenting rejections.


8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sheng-Jen Tsai whose telephone number is 571-272-4244. The examiner can normally be reached on 8:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Sheng-Jen Tsai
Examiner
Art Unit 2186

January 31, 2006


PIERRE BATAILLE
PRIMARY EXAMINER
2/1/06